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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,911	09/17/2003	Frampton E. Ellis III	313449-P0017 C1	2622

47604 7590 09/26/2008

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EXAMINER	
NASH, LASHANYA RENEE	
ART UNIT	PAPER NUMBER
2153	
MAIL DATE	DELIVERY MODE
09/26/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/663,911	ELLIS, FRAMPTON E.	
	Examiner	Art Unit	
	LASHANYA R. NASH	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the claims filed 17 September 2003. Claims 1-25 are presented for further consideration.

Information Disclosure Statement

The Information Disclosure Statements filed by Applicant have been considered.

Specification

The abstract of the disclosure is objected to because of undue length. Correction is required. See MPEP § 608.01(b). Examiner notes:

(b) A brief abstract of the technical disclosure in the specification must commence on a separate sheet, preferably following the claims, under the heading "Abstract " or "Abstract of the Disclosure." The sheet or sheets presenting the abstract may not include other parts of the application or other material. The abstract in an application filed under 35 U.S.C. 111 **may not exceed 150 words in length**. The purpose of the abstract is to enable the United States Patent and Trademark Office and the public generally to determine quickly from a cursory inspection the nature and gist of the technical disclosure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-21 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shaw et al. (US Patent 5,754,766) in view of Kayssi et al. ('FPGA-Based Internet Protocol Firewall Chip"-retrieved from IEEE), hereinafter referred to as Shaw and Kayssi respectively.

In reference to claim 1, Shaw discloses an integrated circuit apparatus employed for shared computer processing (abstract). Shaw explicitly discloses:

- An apparatus comprising (column 6, lines 37-41):
- a personal computer (column 6, lines 41-46; Figure 6-item 108) being configured to provide a wireless network connection (column 13, line 61-column 14, line 3; Figure 6-"wired or wireless interconnection techniques") to a network of said personal computers, the network including an Internet (column 1, lines 42-50);
- the personal computer being further configured to initiate a computer processing operation shared with at least one other said personal computer, and the personal computer also being configured to execute a shared computer processing operation initiated by the at least one other personal computer (column 6, lines 54-66);
- the personal computer including a microchip (i.e. single chip implementation) including a microprocessor with at least a control unit and at least one processing unit, the control unit being configured to allow a user of the personal computer to control the at least one processing unit (column 32, lines 40-52);

- the microchip including a non-volatile memory component; the microchip including a power management component; and the microchip including active configuration of at least one circuit integrated into the microchip (column 32, line 57-column 33, line 5; Figure 9).

However, the reference fails to disclose the microchip including a firewall configured to permit access by the at least one other personal computer through the network to the least one processing unit to execute the shared computer processing operation initiated by the at least one other personal computer. Nonetheless, this would have been an obvious modification to the apparatus of Shaw to one of ordinary skill in the art at the time of the invention, as further evidenced by Kayssi.

In an analogous art, Kayssi discloses an internet protocol firewall chip (abstract). Kayssi further discloses the microchip including a firewall (*2. Chip Overview*, paragraph 1, page 317) configured to permit access by the at least one other personal computer through the network to the least one processing unit to execute the shared computer processing operation initiated by the at least one other personal computer (*1.Introduction*, paragraph 1, page 316). One of ordinary skill in the art would have been so motivated to accordingly modify the apparatus of Shaw so as to include hardware-based firewall to the aforementioned microchip thereby preventing the dangers of the external network (i.e. Internet) from spreading to an internal network (*1. Introduction,* lines 4-10).

In reference to claim 2, Kayssi shows the apparatus wherein the firewall is configured during the shared computer processing operation to deny access to the at least one processing unit by the control unit and to the control unit by the at least one other personal computer (*1. Introduction*, paragraph 1, page 316).

In reference to claim 3, Kayssi shows the apparatus wherein the firewall is a hardware firewall (*1. Introduction*, paragraph 2, pages 316-317).

In reference to claim 4, Shaw shows the apparatus wherein the microchip includes a control and processing unit (column 32, lines 53-67).

In reference to claim 5, Kayssi shows the apparatus wherein the active configuration is provided by the use of field-programmable gate arrays (FPGAs), (abstract).

6. The apparatus of claim 1, wherein the active configuration is provided by the use of a micro electromechanical system (MEMS).

In reference to claim 7, Kayssi shows the apparatus wherein the active configuration is used to configure said firewall (2.*Chip Overview*; paragraph 1, page 317).

In reference to claim 8, Shaw shows the apparatus wherein the control unit is controlled by the use of a remote controller (column 6, lines 58-66; column 32, lines 40-56).

In reference to claim 9, Shaw shows the apparatus wherein the personal computer includes one or more of a telephone, a radio, a pager, a handheld personal digital assistant, a wearable computer, a digital signal processor, an entertainment device, a game, a videocam, an optical data recording device, a camera, a household electronic device, a business electronic device, and an automobile (column 6, lines 44-46; column 32, lines 40-52).

In reference to claim 10, Shaw shows the apparatus wherein the personal computer is configured to establish a direct wireless connection to the at least one other personal computer within a local cluster of personal computers (column 6, lines 58-66).

In reference to claim 11, Shaw shows the apparatus wherein the microchip includes more than one said processing units (column 1, lines 42-45; column 32, lines 57-67).

In reference to claim 12, Shaw shows the apparatus wherein the microchip includes a network communications component (column 33, lines 1-5).

In reference to claim 13, Shaw shows the apparatus wherein the microchip includes a flash memory component (column 32, lines 57-67).

The reference to claim 14, Shaw shows the apparatus of claim 1, wherein the flash memory component includes a BIOS (basic input/output system) of the personal computer (column 33, lines 45-52).

In reference to claim 15, Shaw shows the apparatus wherein the microchip includes a sound component of the personal computer (column 32, lines 40-52).

In reference to claim 16, Shaw shows the apparatus of claim 1, wherein the microchip includes a graphics component of the personal computer (column 6, lines 40-46; column 32, lines 40-52).

In reference to claim 17, Shaw shows the apparatus wherein the microchip includes a video processing component of the personal computer (column 6, lines 40-46; column 32, lines 40-52).

In reference to claim 18, Shaw shows the apparatus wherein the microchip includes an analog component of the personal computer (column 6, lines 63-67).

In reference to claim 19, Shaw shows the apparatus wherein the microchip includes a modem component of the personal computer (column 6, lines 63-67).

In reference to claim 20, Shaw shows the apparatus wherein the personal computer includes more than one said microprocessors (column 1, lines 42-45; column 32, lines 57-67).

In reference to claim 21, Shaw shows the apparatus wherein the personal computer includes at least four said microprocessors (column 1, lines 42-45; column 32, lines 57-67).

In reference to claim 24, Shaw shows the apparatus wherein the network includes a World Wide Web (column 1, lines 16-23).

In reference to claim 25, Shaw shows the apparatus wherein the network includes an Intranet (column 1, lines 42-50).

Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shaw and Kayssi as applied to claim 1 above and further in view of Chin et al. (US Patent 5,497,465), hereinafter referred to as Chin.

In reference to claims 22 and 23, Shaw and Kayssi fail to disclose the apparatus of claim 1, wherein the personal computer includes at least sixteen said

microprocessors [claim 22] and at least sixty-four microprocessors [claim 23]. Nonetheless, this would have been an obvious modification to the apparatus of Shaw and Kayssi for one of ordinary skill in the art at the time of the invention, as further evidenced by Chin.

In an analogous art, Chin discloses a parallel processing system which employs a processing chip (abstract). Chin further discloses wherein the personal computer (i.e. chip) includes at least sixteen said microprocessors (i.e. 64 processors), (column 10, lines 30-46). One of ordinary skill in the art would have been so motivated to accordingly modify the apparatus of Shaw and Kayssi so as to improve operation speed and accuracy for higher speed computing (Chin; column 3, lines 45-54).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LASHANYA R. NASH whose telephone number is (571)272-3957. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenton Burgess can be reached on (571) 272-3949. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LaShanya R Nash/
Examiner, Art Unit 2153
September 7, 2008

/Ario Etienne/
Supervisory Patent Examiner, Art Unit 2157